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			COLEMAN, WILLIAM D	
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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 04172004

Application Number: 09/883,883

Filing Date: June 18, 2001

Appellant(s): BRENNAN, WILLIAM S.

Terry D. Morgan
Reg. No. 31.181
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 16, 2004.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

No amendment after final has been filed.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: The appellant has changed the Examiner's rejection from a 35 U.S.C. 102(e) rejection to a 35 U.S.C. 102(a) rejection.

(7) *Grouping of Claims*

Appellant's brief includes a statement that claims 1-15 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) *ClaimsAppealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

2002/0006677 A1 Egermeier et al. 01-2002

(10) *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14 and 15 are rejected under 35 U.S.C. 102(e).

This rejection is set forth in prior Office Action, Paper mailed August 13, 2003.

Claims 3 and 4 were rejected under 35 U.S.C. 103(a) as being unpatentable over

Egermeier et al.

1. Claims 1, 2, 5, 6, 7, 8, 9, 10, 11, 12 13, 14 and 15 rejected under 35 U.S.C. 102(e) as being anticipated by Egermeier et al., U.S. Patent Publication No. 2002/0006677 A1 4.
2. Egermeier teaches a semiconductor process as claimed. See FIGS. 1-8. Pertaining to claim 1, Egermeier teaches a process for use in fabricating an integrated circuit, comprising: performing an operation on a wafer using a fabrication tool 300; generating desorbed volatiles from the wafer after performing the operation [0023]; sampling the desorbed volatiles; generating raw spectral data from the sampled desorbed volatiles, the raw spectral data indicating the content of the desorbed volatiles; performing a spectroscopic analysis of the raw spectral data-, and modifying an operational parameter of the fabrication tool responsive to the result of the results of the spectroscopic analysis [0025].

3. Pertaining to claim 2, Egermeier teaches the process of claim 1, wherein performing an operation on a wafer using a fabrication tool includes performing a chemical-mechanical polishing operation, a plasma etching operation, or a wafer cleaning operation (i.e., cleaning encompasses annealing the wafer to remove unwanted materials [0018]).

4. Pertaining to claim 5, Egermeier teaches the process of claim 1, wherein generating desorbed volatiles from the wafer after performing the operation includes heating the wafer in a vacuum chamber to generate desorbed volatiles.

5. Pertaining to claim 6, Egermeier teaches the process of claim 5, wherein heating the wafer in a vacuum chamber includes heating the wafer in a lamp degas chamber or a pedestal temperature controlled process chamber [0033].

6. Pertaining to claim 7, Egermeier teaches the process of claim 1, wherein sampling the desorbed volatiles includes sampling the desorbed volatiles with a residual gas analyzer [0023].

7. Pertaining to claim 8, Egermeier teaches the process of claim 1, wherein modifying the operational parameter includes issuing a new APC plan [0026].

8. Pertaining to claim 9, Egermeier teaches the process of claim 1, further comprising at least one of storing the results of the spectroscopic analysis; performing a trend analysis on the results of the spectroscopic analysis; and performing a variability analysis on the results of the spectroscopic analysis [0029].

9. Pertaining to claim 10, Egermeier teaches a process for use in fabricating an integrated circuit, comprising: receiving raw spectral data representative of the content of a plurality of volatiles desorbed from a wafer; processing the raw spectral data to determine the presence of a

residual material on the wafer; and controlling a process flow operation to reduce the amount of the residual material on the wafer responsive to the results of processing the raw spectral data.

10. Pertaining to claim 11, Egermeier teaches the process of claim 10, wherein receiving the raw spectral data includes receiving the raw spectral data through at least one of a sensor interface and a data handler.

11. Pertaining to claim 12, Egermeier teaches the process of claim 10, wherein processing the raw spectral data includes performing a spectroscopic analysis on the raw spectral data.

12. Pertaining to claim 13, Egermeier teaches the process of claim 10, wherein controlling the process flow operation to reduce the amount of the residual material on the wafer includes modifying an operational parameter of a fabrication tool.

13. Pertaining to claim 14, Egermeier teaches the process of claim 13, wherein modifying the operational parameter includes issuing a new APC plan.

14. Pertaining to claim 15, Egermeier teaches the process of claim 10, further comprising at least one of storing the results of the spectroscopic analysis; performing a trend analysis on the results of the spectroscopic analysis; and performing a variability analysis on the results of the spectroscopic analysis.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egermeier et al., U.S. Patent Application Publication No. US 2002/0006677 A1 as applied to claims 1-2 and 5-15 above, and further in view of Lee et al., U.S. Patent 5,865,900.

16. Egermeier teaches a semiconductor process substantially as claimed as discussed above. However, Egermeier fails to disclose the process of claims 1 and 2 wherein modifying the operational parameter of the fabrication tool includes increasing a rinse time or increasing a polishing time of the chemical mechanical polishing operation or resetting a scheduled maintenance time. Lee teaches modifying the operational parameter of the fabrication tool to include a time function for the chemical mechanical polishing operation. In view of Lee, it would have been obvious to one ordinary skill in the art to incorporate the process steps of Lee into the process of Egermeier because the residual gas analyzer as an endpoint detection step (column 9, line 9) and CMP is common in the art (column 6, lines 60-61).

(11) Response to Argument

Applicant contends that Egermeier fails to disclose “modifying an operational parameter of the fabrication tool responsive to the result of the results of the spectroscopic analysis,” as recited in independent claim 1 and, hence dependent claims 2-9; and “controlling a process flow operation to reduce the amount of the residual material on the wafer responsive to the results of processing the raw spectral data,” as recited in independent claim 10 and, hence, dependent claims 11-15.

In response to Applicant's contention that Egermeier fails to disclose the limitation "modifying an operational parameter of the fabrication tool responsive to the result of the results of the spectroscopic analysis," as recited in independent claim 1. Please see FIG. 1 which discloses a flow chart for processing a wafer at step 101. At step 110, the process inquires whether or not the wafer is within acceptable contaminant range. In paragraph [0025], Egermeier discloses a decision is made as to whether the wafer (via the effluent data point) is within the baseline (which includes a general purpose computer system as disclosed in [0023 & 0024].

The Examiner takes the position that "modifying an operational parameter of the fabrication tool responsive to the result of the results of the spectroscopic analysis," as recited in independent claim 1 as recited by Applicant is equivalent to FIG. 1 and the computer system and residual gas analyzer in the Egermeier disclosure.

Applicant contends Egermeier fails to disclose "controlling a process flow operation to reduce the amount of the residual material on the wafer responsive to the results of processing the raw spectral data" as recited in independent claim 10 and, hence, dependent claims 11-15.

In response to Applicant's contention that Egermeier fails to disclose "controlling a process flow operation to reduce the amount of the residual material on the wafer responsive to the results of processing the raw spectral data" as recited in independent claim 10 and, hence, dependent claims 11-15. The Examiner takes the position that FIG. 1 reads on Applicants limitations of claim 10. Please note at step 108, Egermeier discloses comparing analysis in real

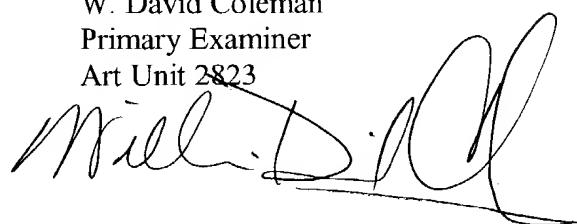
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time (raw data) to base-line data points and in step 110, Egermeier discloses either continue to process the wafer (one controlling process flow operation) or rejecting the wafer (step 112).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

W. David Coleman
Primary Examiner
Art Unit 2823



WDC
April 17, 2004

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